REMARKS

Applicants respectfully request reconsideration and allowance of all claims in the Application in view of the following remarks. In the Office Action, the Examiner rejects claims 1-3, 7, 8, 14-29 as anticipated by U.S. Patent no. 6,595,707 to Kuwata ("Kuwata") under 35 U.S.C. § 102(e). Claims 27-42 are allowed and claims 4-6 and 9-13 are identified as containing allowable subject matter.

Allowed Claims and Allowable Subject Matter

Applicants thank the Examiner for acknowledging the allowability of claims 27-42 and the allowable subject matter of claims 9-13. However, Applicants respectfully submit that independent claim 1 is also allowable and that no amendment to claims 9-13 is required at this time.

Rejections under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a)

Kuwata does not anticipate the claims of the present Application as alleged in the outstanding Office Action. A cited prior art reference anticipates a claimed invention under 35 U.S.C. §102 only if every element of the claimed invention is identically shown in the single reference, arranged as they are in the claims. MPEP §2131; *In re Bond*, 910 F.2d 831, 832, 15 USPQ 2d 1566, 1567 (Fed. Cir. 1990). Kuwata does not teach or suggest, *inter alia*, aspects of parity calculation that are required in the present claims.

For example, independent claim 1 requires a parity module configured to receive certain input bits from one of the binary number sequence and a previous column and to calculate the parity of the certain input bits. Kuwata does not teach or suggest a parity module or the calculation of parity of input bits. The word parity does not appear in Kuwata. Kuwata is directed to a code conversion circuit having a bit distributing unit for dividing a high speed input signal into N ways of low speed signals. Kuwata, Abstract. In Kuwata's code conversion circuit:

> N number of pre-coders (or decoders), each comprised of an EXOR circuit 15, a delay element 16 (often not existing as actual element) and a D-FF circuit shown in FIG. 19, are provided in parallel. Considering the case where N=2 and the above example, the strict restriction of the delay time Td having to be less than 100 ps at all times is tremendously eased to the restriction of keeping Td less than 200 ps. If N=4, the restriction is eased to keeping it less than 400 ps.

Kuwata, col. 7, lines 22-31. Kuwata is concerned with easing timing restrictions – not with calculating parity – and, consequently, the absence of parity modules or parity calculations of

input bits in the Kuwata specification and drawings is unsurprising. Moreover, even if Kuwata can be said to discuss or mention certain of the components that are recited in certain of the claims (e.g. exclusive-OR logic elements), Kuwata does not teach these elements arranged in any manner that anticipates the claimed subject matter. Therefore, Kuwata cannot be said to identically show all elements of independent claim 1, arranged as they are in the claim and the rejection of independent claim 1 and its dependent claims should be withdrawn.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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